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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,866	05/16/2002	Edwin Fauser	10191/2052	8917

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EXAMINER

BENENSON, BORIS

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/030,866	Applicant(s) FAUSER ET AL.	
	Examiner Boris Benenson	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17-25, 33 and 34 is/are rejected.
- 7) ☒ Claim(s) 26-32 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10.18/2001</u> . | 6) <input type="checkbox"/> Other: _____ |

Detailed Actions

1. Preliminary Amendment received On 05/16/2002 is entered. Claims 1-16 are cancelled. A set of new Claims 17-34 is entered. Substitute Specification is entered.

Claim Objections

2. Claim 27 objected to because of the following informalities: On line of the Claim instead of words "to the" appears combination "to the" (mistyped). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 17,22-25 and 34 are rejected under 35 U.S.C. 102(a) as being anticipated by Arledge et al. (6,493,198). Arledge et al. disclose an Electrostatic Discharge Protection Device For A High Density Printed Circuit Board. The device is designed to

Art Unit: 2836

protect a Printed Circuit Board (PCB) from ESD due "the physical contact or handling by a person of a product containing ESD sensitive electronic components" (Col.1, Lines 17-19). The device comprises a first electro-conductive structure (Fig.3, Pos. 50) carrying various signals of the electronic device and a second electro-conductive structure (10) - a ground conductor / trace or ground plane that is disposed on a dielectric substrate. "An aperture or via (40) is formed in the dielectric layer (30) so that a portion (15) of the ground conductor (10) is exposed" (Col.2, Lines 44-46). "A portion 52 of the trace is disposed near the via 40 to create a spark gap that provides for discharge paths between the circuit trace and the ESD conductive grounding pattern" (Col.2, Lines 58-61). It is inherent that the first and the second structure conductively connected to contact elements such as pads or pins on order to be connected to a power source or to input/output circuitry.

Referring to Claims 22 and 24, Arledge et al. disclose a multi-layer substrate wherein "a ground conductor or ground plane (10) is disposed on a dielectric substrate (20)" (Col.2, Lines 31-33), "one or more circuit conductors generally indicated by the reference numeral 50 are disposed on top of the layer of dielectric material 30" (Col.2, Lines 50-52), an aperture or via (40) read on a blind opening is provided in a

Art Unit: 2836

circuit trace (50) and an insulating plane (30) so bottom of the opening is formed by second circuit trace, and a spark discharge is taken place in a gap formed by the blind opening between an inner wall section of the printed circuit trace and the bottom of the opening.

Referring to Claim 23 and 25, the second printed circuit trace (10) includes a large area earth plane (15) of the multi-layer substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this

Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arledge et al. (6,493,198) in view of Fong et al. (5,315,472). Arledge et al. disclose an Electrostatic Discharge Protection Device For A High Density Printed Circuit Board that includes all elements of independent Claim 17, as it

was discussed above. Arledge et al. did not disclose the first and the second electro-conductive printed traces configured on a shared surface of the substrate and the first and the second structures have mutually facing projections that are separated from each other by the gap. Fong et al. teach a Ground Ring / Spark Gap ESD Protection Of Tab Circuits. Fong et al. teach spark gap (Fig.4E, Pos. 23a, 23b) between traces (17a and 19) formed on a surface of a substrate wherein mutually faced projections are separated by the gap. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Arledge et al. with teachings of Fong et al., because it provides an ESD protection without necessity to create a multiplayer structure on the substrate.

Referring to Claims 19 and 20, Arledge et al. disclose (Figure 1) mutually facing projections of the traces taper and have included mutually pointed ends.

Regarding to claim 21, even though the claims are limited by and defined by the recited process, the determination of patentability of the product is based on the product itself, and does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*,

Art Unit: 2836

227 USPQ 964, 966 (Fed. Cir. 1985). The device of Claim 18 will function regardless of using a laser cutting or different method of producing the gap between the projections.

5. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arledge et al. (6,493,198) in view of Fischer (5,034,801). Arledge et al. disclose an Electrostatic Discharge Protection Device For A High Density Printed Circuit Board that includes all elements of independent Claim 17, as it was discussed above. Arledge et al. disclose also that "The spark gaps prevent the potential differences between adjacent interconnects from exceeding a defined limit range known to be safe for the circuitry interconnected by the interconnect circuitry and generally determined by the gap size" (Col.3, Lines 26-30). In other words the size of spark gap should be determine by voltage determine to be safe for electronic components of protected circuitry. The minimum size of the gap is shown on Fig. 2 as a thickness of a dielectric layer (30). Arledge et al. did not disclose the thickness of the dielectric layer (30). Fischer teaches Integrated Circuit Element Having A Planar, Solvent-Free Dielectric Layer. Fischer teaches, "The dielectric layer has a thickness of 25 micrometers or less" (Col.2, Lines 67-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

Art Unit: 2836

have modified Arledge et al. and create a dielectric layer with a thickness of 25 micrometers or less as teaches Fischer if a component safety consideration require a spark gap of such size.

Allowable Subject Matter

6. Claims 26-29 and 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reason for indicating Allowable Subject Matter

7. Claim 26 would be allowable because none of the prior art of record disclose an ESD protection device wherein an spark gap between a traces located on different layers produced by a bore hole penetrating the multi-layer substrate in combination with the other claim limitations.

8. Claim 27 and 28 would be allowable because none of the prior art of record disclose an ESD protection device that includes conductor element that project from the carrier substrate and the end of the conductor element not connected to the carrier substrate separated from a second printed trace on

Art Unit: 2836

the carrier substrate producing a spark gap in combination with the other claim limitations.

9. Claims 30 would be allowable because none of the prior art of record disclose an ESD protection device wherein the mutually facing sections of the printed circuit traces and the gap are covered by at least one of an active component and a passive electrical component in combination with the other claim limitations.

10. Claims 29, 31 and 32 are dependent on Claims 28 and 30 and would be if Claims 28 and 30 were allowed.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Art Unit: 2836

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Boris Benenson
Examiner
Art Unit 2836

B.B.

A handwritten signature in black ink, appearing to read 'Brian Sircus', with a stylized, sweeping flourish extending from the end of the name.

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800